Low Temperature Polysilicon Technology for Advanced Display Systems

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Abstract

In this paper I review research and development in the area of low temperature polysilicon (p-Si) formation for application in advanced display systems. A brief introduction to the scope of these efforts and the market for this technology is given, followed by a presentation of the methods that are being developed to meet these objectives. The technical merits and demerits of various approaches for low-temperature p-Si formation are reviewed on the basis of current studies, and an attempt is made to extrapolate trends and suggest solutions for the technical difficulties that currently plague the development of a manufacturing-compatible process.

Introduction

Over the past 25 years, LCD technology has significantly evolved and presently holds a dominant position in high information-content flat panel displays (FPDs). Since the beginning, in the early 80s, visionary researchers and prudent manufacturers have been constantly seeking for ways to increase panel size, improve performance and reduce costs associated with the manufacture of TFT-LCD. In the 80s, such a performance improvement was achieved by the transition from passive TN displays to passive supertwisted nematic (STN) and subsequently to active-matrix a-Si TFT-LCDs. Forced by market demands, and fueled by technological breakthroughs and a need to effectively utilize older generation a-Si manufacturing lines, a similar transition is seen in the mid-90s to occur, whereupon low-temperature polysilicon (LPS) emerges as a feasible substitute for the mature a-Si technology.

Compared to amorphous silicon, polysilicon offers significantly higher carrier (electron & hole) mobility. As a result of the higher carrier mobility, several improvements are possible: (a) device dimensions can shrink allowing for higher aperture ratio, increased brightness and/or reduced power consumption; (b) higher pixel driving TFT "on" current, resulting in less sensitivity to RC delay time and large reduction in the pixel charging time; this, facilitates wider gray scale, color and real-time video. (c) Monolithic integration of CMOS drivers and other circuit elements enabling thinner form factor, lighter weight and, potentially, higher reliability and lower cost.

Monolithic integration is of particular importance, given the fact that driver circuitry accounts for 5-30% of the total panel cost. Fabricating the drivers directly on the glass, eliminates the traditional

driver "attachment" and "packaging" steps, simplifies the assembly of the module and slashes module assembly equipment costs. Thus, assembly yield is increased and, moreover, panel process throughput and reliability are increased, as fewer external interconnects are required. One can envision the integration of not only the CMOS drivers, but of an array of other elements (controller, memory, specific ICs) once a reliable, mature LPS process is established. With this addition, the panel becomes the system itself leading to the era of the SOP (system-on-panel) concept that Sharp has long envisioned and is aggressively pursuing.

Low temperature polysilicon technology has been intensively investigated for at least the past 15 years for application in LCDs. Conventional high-temperature polysilicon processing (>900˚C) requires quartz substrates that are too expensive, except for very small display sizes (<1.5" dia.). LPS technology aims at using standard, less expensive glass substrates (sized currently up to 550 x 650mm^2). Such substrates are available from all major glass manufacturers, at projected price levels similar to these for a-Si technology.

The immediate market for LPS technology seems to be in the small to medium-sized (3" to 8") display. According to recent press releases and other announcements, these panels are expected to appear in products such as projectors, camcorders (viewfinders or view-cam displays), car navigation systems, digital cameras, PDAs, etc. **(table 1)**. Undoubtedly, these markets are not sufficient to sustain a healthy LPS technology. It seems, however, that manufacturers consider this type of markets as the criterion of success for LPS and the means to debug and improve the technology before migrating to larger panel sizes. Data from a recent report by DisplaySearch indicate that LPS technology can enjoy a cost advantage in display sizes up to 14" XGA with full driver and panel ASIC integration.[1)] Moreover, recent moves from LCD panel manufacturers, such as Toshiba and Sony (among others), indicate that manufacturing of notebook displays and LCD monitors, based on low-temperature polysilicon technology, may not be as far as it was thought, not-so-long time ago.

Table 1 LPS Display and Application.

Company	Display	Application
Sharp	4.5"VGA	PDA
Sanyo	2"(521 X 218)	Dig.Camera
Sony	1.8"(800 X 225)	Dig.Camera
Toshiba	12.1"	PC
Fujitsu	3"-5"	Projector

Despite the advantages and the potential cost reduction, LPS must overcome a number of manufacturing challenges to reap these benefits. First and foremost, all processing must be conducted at temperatures lower than 450-500˚C or, equivalently, at a thermal budget compatible with low-cost standard glass. Furthermore, equipment for the additional and/or modified processes, such as reduced H-content silicon deposition, crystallization, ion-doping, gate dielectric film formation, hydrogenation and finer resolution lithography tooling need to be introduced and optimized for 3rd and higher display generations.

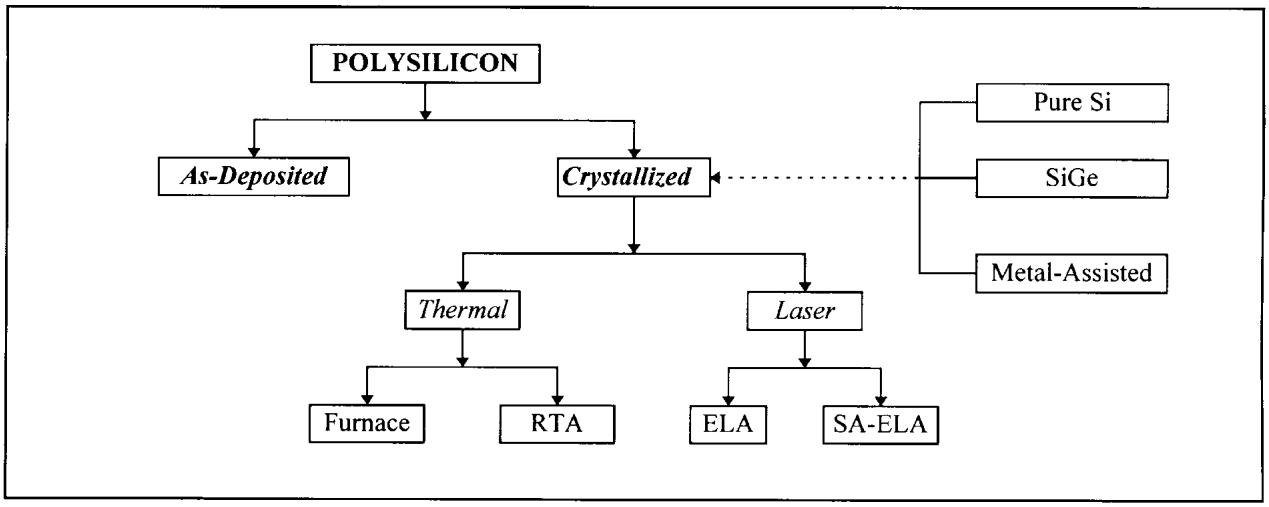

Fig. 1 p-Si formation techniques.

The performance of polysilicon TFTs is a function of several material, process and device parameters. The material parameters, in turn, depend upon the method that is chosen to form the polysilicon film. This article focuses on research on the formation of polysilicon at low temperatures. In the following, a number of approaches that have been developed towards this objective are discussed. The technical merits and demerits are reviewed on the basis of current experience, and an attempt is made to extrapolate trends and suggest solutions for the technical difficulties that currently plague the development of a manufacturing-compatible process.

1. Active Layer Formation Techniques

In general, there are two fundamental ways to form polycrystalline silicon films: (1) deposition of the silicon film directly in the polycrystalline phase (referred to as as-deposited polysilicon), and (2) phase transformation to polysilicon (referred to as crystallized polysilicon) by means of a crystallization step, whereupon some form of energy (thermal energy, phonon energy) is supplied to the as-deposited silicon film to accomplish the phase transformation. **Fig. 1** illustrates the different approaches for the formation of polysilicon films.

1•1. Microstructure of as-deposited silicon films

In general, the microstructure of as-deposited silicon films is determined by the balance between the incident atom flux and the surface mobility of the adsorbed surface species. When conditions are such as the former rate is much larger than the surface mobility of the species, an amorphous-like structure will develop. In contrast, in the opposite case, a polycrystalline structure will be favored.[2]

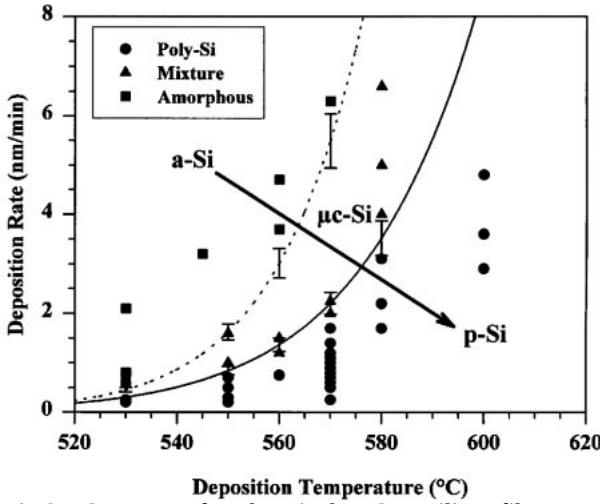

Fig. 2 Structure of as-deposited LPCVD silicon films as a function of temperature and deposition rate.[3]

Fig. 2 shows a phase diagram for the case of as-

deposited LPCVD silicon films. The two familiar structure regimes can be easily discerned (amorphous and polycrystalline phases), separated by a third regime where a mixed-structure (crystallites embedded in an amorphous matrix) is obtained. As shown in **fig. 2**, a transition from amorphous to polycrystalline silicon is observed to occur, through this mixed-phase regime, as the deposition temperature increases and/or the deposition rate decreases.

In a previous work we have identified the surface diffusion length of silicon adatoms to provide a good, quantitative measure of the expected size of crystalline growth in as-deposited LPCVD films.[2) 3)] For silicon deposition from silane gas, we have derived an analytical expression for the expected crystallite size, which is plotted in **fig. 3** along with experimental data.[3)] The data trend indicates that the size of crystallites should be expected to decrease at higher deposition rates, as it is intuitively expected from thermodynamics and kinetics considerations. Even though this model has been derived for thermal CVD of silicon films based on silane chemistry, similar results can be obtained for other deposition methods and alternative chemistries upon substitution of appropriate expressions for the deposition rate and surface diffusivity in eq. (1).

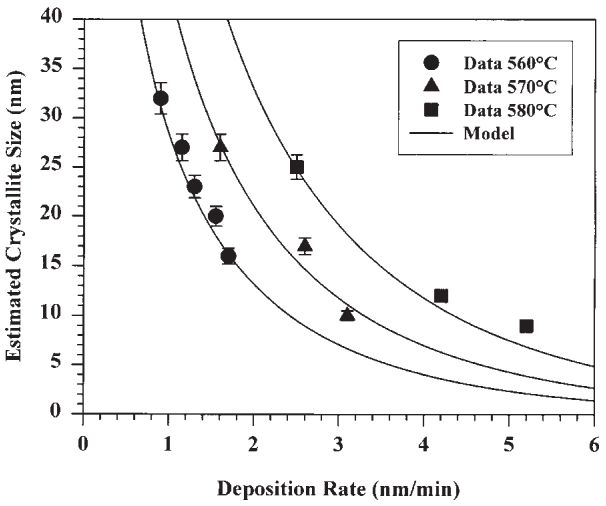

Fig. 3 **Crystallite size of as-deposited S-films versus temperature and deposition rate.**

$$L_{cr} = \sqrt{\frac{d \cdot D_{ss}}{R}} \qquad (1)$$

where, Lcr is the crystallite size, d is the thickness of one monolayer of Si, Dss is the surface diffusivity of silicon species and R is the deposition rate.

In fact, control of the phase of as-deposited silicon films has been achieved, to a certain degree, with a variety of deposition techniques such as plasma-enhanced CVD, photo-CVD and, more recently, sputtering and hot-wire CVD.

1•2 As-deposited polysilicon

Deposition of silicon directly in the polycrystalline phase is the ultimate goal as far as simplicity and cost reduction. However, before such a process is widely adopted, there are certain problems that deserve consideration. The first problem relates to film quality: the microstructure of as-deposited polysilicon films, in terms of grain size and defect density, tends to be of inferior quality. This is the consequence of two main trends: (i) reduction of the thermal budget to achieve compatibility with standard glass substrates, (ii) increase of the deposition rate to boost process

throughput. Both effects are detrimental to the structural characteristics of the films, resulting in poor electrical performance. An additional problem with as-deposited polysilicon films is the typically increased surface roughness, which tends to cause surface scattering at the insulator/polysilicon interface and degrade the performance of the TFT device.
Despite the problems associated with as-deposited polysilicon, particular emphasis has been placed in its development due to the significant payoff from such a process. Currently, research efforts emphasize on the following areas:

a) Chemical or physical modification of the substrate to allow for improved "wetting" of the silicon to eliminate surface roughness. Introduction of suitable under-layers (typically thin metal films) may prove to be an alternative way to achieve this objective.
b) Low-temperature, controlled gas phase decomposition to yield silicon species with maximum surface mobility. This concept seems to underline efforts associated, among others, with the so-called hot-wire deposition method.
c) Reduction of background contaminants by adding ultra-high-vacuum capability to deposition chambers. According to our previous studies, reduction of the background levels of oxygen and water vapor can both increase the grain size and reduce the intra-grain defect density.

Table 2 summarizes the structural improvements in LPCVD as-deposited polysilicon films, deposited at 570˚C, as a function of various treatments. As shown, a significant improvement in all of the structural characteristics is observed by employing a substrate cleaning step and utilizing a low background oxygen deposition chamber. Reduction of the deposition rate is shown to improve surface roughness by allowing ample time for surface diffusion before 3-dimensional clusters form and "freeze" on the growing surface.

Table 2 Effect of various treatments on LPS quality.

Treatment	Dep. Rate (Å/s)	Grain Size (nm)	Defect Density (cm^{-2})	Surface Rough. (nm)
No Clean	17	25	5e13	1
Clean	17	57	3e13	9
Clean	6	86	8e12	5
Clean/Low-O_2	6	100	2e12	3

1•3 Crystallized polysilicon

As shown in figure 1, crystallized polysilicon can be formed by a variety of processes. Variations include not only the method chosen for the phase transformation, but the deposition technique itself, the choice and method of introduction of impurities acting as "catalysts" during crystallization, etc. As we will discuss, the deposition method and all other measures are intimately related to the technique that is chosen to anneal the as-deposited films. As a result, we have chosen to discuss this subject under the broad classification of laser-annealed polysilicon and non-laser annealed polysilicon.

1•3•1 Excimer laser annealed (ELA) polysilicon

ELA process is currently one of the most potent techniques for adoption to manufacturing. From the research point of view, very high quality polysilicon has often been reported in the literature with TFT mobility values ranging in the 100cm^2/Vs to >300cm^2/Vs range. The main advantages of ELA process are: (i) crystallization from the melt, resulting in high quality, almost defect-free, large grains, and (ii) compatibility with low-cost glass substrates. On the flip side, several disadvantages have also been noted: (i) high-cost process, (ii) typically narrow operating window which increases operating costs, undermines throughput and makes the process susceptible to equipment variations. (iii) Inherent variability in the materials characteristics due to the scanning nature of the beam, whereupon successive beam shots overlap, to a degree, to form a continuous pattern. (iv) Pulse to pulse variability, (v) equipment maintenance costs, and, (vi) often substrate damage are other problems related to ELA process.

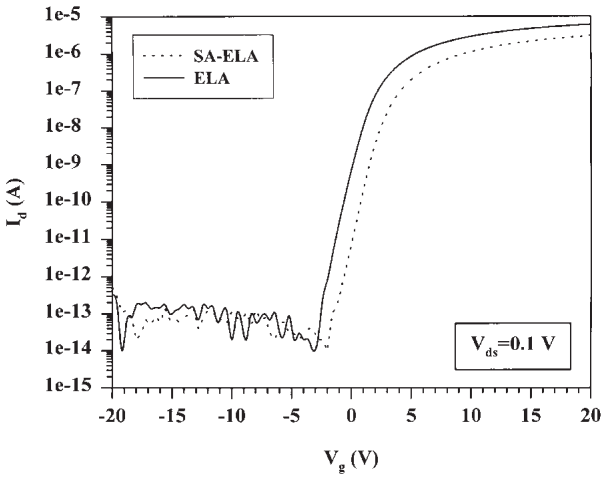

Fig. 4 I_d -V_g Characteristics for p-Si TFTs.

Table 3 Laser-Annealed p-Si TFT characteristics

Method	m (cm^2/Vs)	Vth (V)	S (V/dec)
SA-ELA	61	4.6	0.7
ELA	123	3.1	0.7

Generally, ELA process is conducted in high vacuum, with the substrate heated at a temperature in the range of 300-400˚C. A different approach has been introduced by a French equipment maker, SOPRA, where the laser anneal is conducted in air and room temperature via the so-called Single-Area ELA process, whereupon an area as large as 8x8in^2 is annealed with one shot. This process is claimed to result in improved equipment reliability and lower maintenance and consumable costs due to the significantly lower number-of-shots requirement. Moreover, due to the lack of overlap, better uniformity in the post-annealed materials characteristics is implied. **Fig. 4** shows I_d-V_g characteristics of poly-Si TFT devices fabricated by standard ELA and by SA-ELA processes. **Table 3** compares the key TFT characteristics.

The mobility of SA-ELA p-Si TFTs has been found repeatedly to be inferior to that of ELA p-Si TFTs. Despite the reduced mobility, however, threshold voltage and subthreshold swing have been found to be comparable, at optimum conditions, between the two methods. We believe that the reduced mobility is the result of increased grain boundary trap density in the case of SA-ELA films. The reason for that is not fully understood yet, but we hypothesize that it may be related to the choice of precursor material (i.e. deposition method) and annealing conditions (i.e. anneal in air). It has been shown that mobility values in the range of 100cm^2/Vs can be obtained by utilizing

LPCVD silicon as the precursor material.

Clearly, during optimization of p-Si formation, both deposition and annealing processes have to be given equal weight. The deposition process that works well with annealing process "A" may not necessarily be optimum for annealing process "B". With this in mind, we developed and optimized a new PECVD Si-precursor material for ELA formation of polysilicon. In this case the silicon film is deposited in the microcrystalline phase, having a controlled density of crystallites embedded in an amorphous matrix. Our results indicate that upon laser anneal a twofold increase in the grain size of the polysilicon film can be obtained by utilizing this type of silicon precursor. Alternatively, with this type of material high quality polysilicon can be formed at reduced levels of energy density, allowing for wider process margin and improved equipment reliability. Moreover, this type of film may be more compatible with the SA-ELA approach.

The current main focus in ELA related research can be best summarized as: "in search of the right precursor". Particularly, the ideal precursor should have all of the following properties: (i) capable of large area deposition (550x650 mm^2) with good uniformity (<±7%) and high deposition rate (>5Å/min) (ii) no need for dehydrogenation, (iii) wide process margin (i.e. invariant to pulse-to-pulse variability), (iv) good crystalline uniformity (i.e. invariant to laser beam overlap). (v) Moreover, the film cost should be low and the process unsaturated (i.e. compatible with future modifications and additional requirements). We are currently working towards finding such a precursor and aid in the selection of the future LPS process.

1•3•2 Non-ELA, low-thermal-budget polysilicon

Historically, the development of low temperature polysilicon has its roots in solid phase crystallization processes, mainly conducted in diffusion furnaces. Due to a compromise, however, between annealing time, annealing temperature and film quality, the thermal budget of the process tends to exceed the limit imposed by the glass substrate. Several methods have been proposed in the literature to remedy the problem, ranging from utilizing composite films, with one layer providing nucleation seeds and the other layer amorphous material for consumption, to employing various alloys to enhance the silicon crystalline growth at low temperatures and, thus, reduce the annealing time. Such examples can be drawn from the use of SiGe as the semiconductor material as well as the so-called silicide-mediated crystallization, whereupon a silicide is rapidly formed at low annealing temperatures (300-400˚C) and subsequently catalyzes the crystallization of silicon upon further anneal at a higher temperature (>500˚C).

Recently, another technique has emerged as a promising candidate for application in the flat panel displays. This technique, Rapid Thermal Annealing, has been brought in the area of FPDs by a US company, Intevac. The main advantages of the RTA process are: simplicity, fast processing and low capital cost. On the other hand, film quality and compatibility with the glass substrate are still issues under investigation. Furthermore, the adaptability of this technique to future requirements,

and its compatibility with new types of substrates (i.e. polymer-based substrates) with even lower thermal budget requirements is, as a minimum, questionable. In spite of these issues, however, aggressive development is under way to bring this process to manufacturing, since in addition to the reasons mentioned above, RTA can be also used in steps other than crystallization (such as dopant activation, gate insulator densification), making it a desirable tool for the factory floor.

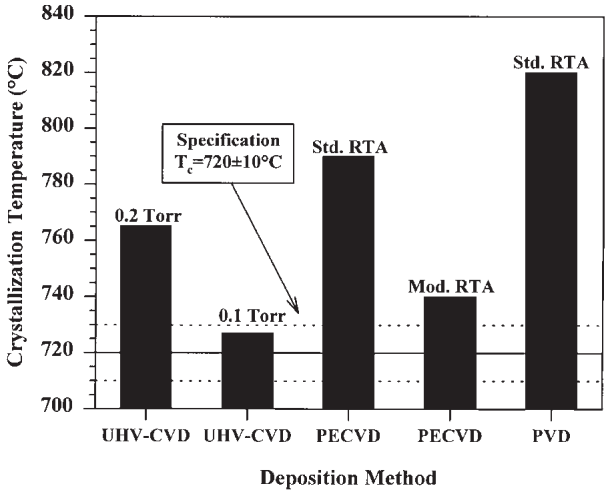

Fig. 5 Crystallization temperature for RTA Si-films

The selection of precursor silicon material is even more important in the case of RTA. The crystallization threshold of different silicon films can vary quite widely as evidenced by the data of **figure 5**. The new generation of glass substrates (such as the 1737 Corning glass) provide for higher strain points that the previous glasses, optimized for a-Si technology. However, in order to maintain a safe process margin, the crystallization temperature during RTA has to be within the range of 720 ±10˚C. This poses a significant difficulty in establishing a reliable and reproducible RTA crystallization process. Combination of RTA process with some of the alloying techniques, discussed earlier, may provide a viable alternative for reducing the thermal budget and bringing this process soon to manufacturing.

Conclusion

After everything is said and done, the question still remains: what is the best way to form low-temperature polysilicon? The answer to this seemingly simple question is equally, ostensibly simple: it depends; what is the intended application, what is the future of the technology, what is the type of markets that each manufacturer envisions to capture with his products, what is the real cost advantage against amorphous silicon technology in mature, high volume markets, etc. Looking at the current status of production-worthy LPS technology and making certain assumptions, we have roughly constructed a road-map **(fig. 6)**, where performance requirement (expressed by mobility) for circuit-driving, p-Si TFTs has been placed on a time axis.

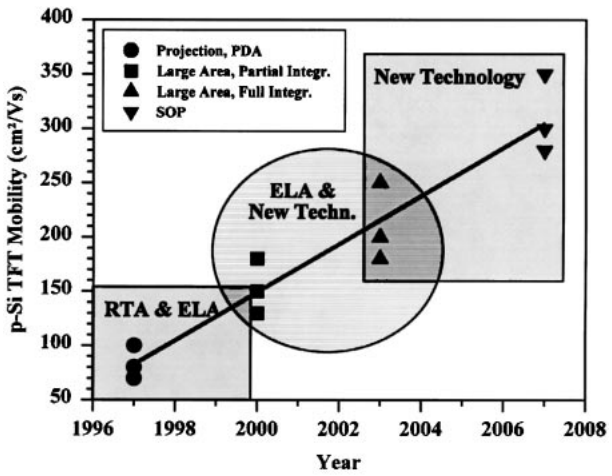

Fig. 6 LPS performance road-map.

According to this road-map, current performance requirements could be satisfied by an optimized

RTA process. As the performance requirement, however, becomes more demanding, it is projected that RTA technology will eventually reach a hard limit. To go beyond that limit, ELA technology will be required; alternatively, it is expected that new technologies, currently at the development stage, will be able to effectively compete with the traditional ELA approach and advance LPS technology to the next level of performance, compatible with system-on-panel (SOP) requirements. These new approaches will aim at providing a better silicon precursor material to match the crystallization process, improving the annealing technique to yield low defect density p-Si material without melting the film and, ultimately, providing ways to eliminate the crystallization step altogether.

References

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